replaced and rewritten. Claims 30 and 31 have been reinstated and amended. New Claims 32 through 38 have been added. The Specification, page 1, has been amended.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of the Specification objected to because of informalities as cited by the Examiner is requested based on the Amended Specification and the following remarks.

A statement regarding the division of the Patent Application has been added as requested by the Examiner.

Reconsideration of the Specification objected to because of informalities as cited by the Examiner is requested based on the Amended Specification and the above remarks.

Reconsideration of Claim 29 rejected under 35 U.S.C. 102(b) as being anticipated by Sakakibara (U.S. Patent 5,691,560) is requested based on Replaced and Rewritten Claim 29 and on the following remarks.

The Applicants agree with the Examiner that the previously written device claims were not sufficiently limited. Their novel device is formed from their novel method as disclosed in U.S. Patent 6,297,098. The claims have been amended and new ones added to reflect the novelty as found in the specification and the original claims. No new matter has been added. These amended claims distinguish this device from the cited prior art.

According to the method a tilt angle implantation is applied twice to the substrate using a formed gate stack having sidewall spacers as an implantation mask. First a light implantation of phosphorous is made at an optimum tilt angle to cause impurities to become situated under the gate stack. Second, a heavy implantation of arsenic, also made at an optimum tilt angle, causes the impurities to become situated beneath the sidewall spacers. In the disclosed device, this tilt angle implantation is applied only to the drain region of the device, where the source region had previously been formed and is protected from further implantation. The drain is formed in a region common to two memory cells. A short time (10 to 20 minutes) of diffusion of the strategically placed implnated light and heavy dopants forms a smooth graded dopant profile well beneath the stacked gate. This smooth profile provides a

reduced electric field during operation such that hot carrier effects are precluded, providing optimum conditions for well behaved junctions, resulting in increased program speed, reduced program current, increased read current and reduced drain disturb voltage.

Independent Claim 29 has been overhauled such that the Applicants respectfully request that old Claim 29 be replaced with a newly written Claim 29. Previously, Claims 30 and 31 had been canceled to amend the original Claim 29. However, those limitations no longer reside in the new Claim 29 and the Applicants respectfully request that Claims 30 and 31 be reinstated together with new amendments. The Applicants also respectfully request that new Claims 32 to 38 be accepted. These new dependent Claims 32 to 38 do not present new matter, but provide further limitations on the preferred embodiment.

Regarding Claim 29, the novelty of the invention is in the smoothly graded profile of the junction involving the drain that limits the electric field and the attendant problems. This results in a device that exhibits desirable threshold voltages and presenting a minimum disturb voltage difference condition. This device is described by these characteristics. An accurate

description of the drain junction dopant profile is best made by using a partial description of the process.

It is respectfully suggested that these amended claims distinguish the instant invention from the previously cited prior art. Therefore, the Applicants request respectfully that Examiner Pizarro reconsider these rejections in view of these amendments and allow Claims 29 through 38.

Reconsideration of Claim 29 rejected under 35 U.S.C. 102(b) as being anticipated by Sakakibara (U.S. Patent 5,691,560) is requested based on Replaced and Rewritten Claim 29 and on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and agree with the Examiner that while the references are of general interest, they do not apply to the detailed Claims of the present invention.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner Pizzaro not find that the Claims are now Allowable that he call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,

Douglas R. Schnabel, Reg. No. 47,927

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Please move the statement reading:

"This is a division of Patent Application Ser. No. 09/431,236, filed on 11/1/1999, now U.S. Patent 6,297,098."

to page 1, line 1 of the Specification.

In the Claims:

Please Replace Claim 29 with Rewritten Claim 29 as follows:

29. (AMENDED REWRITTEN) A stacked gate memory cell pair having a graded doubly diffused drain (DDD) profile exhibiting minimum disturb voltage difference comprising:

a semiconductor substrate of a first conductivity type having active and passive regions defined and having a top surface;

a pair of stacked gates overlying the substrate surface, each said stacked gate having a gate oxide layer overlying the substrate, a floating gate layer overlying the gate oxide layer, an inter-gate oxide layer overlying the floating gate, a control gate overlying the inter-gate layer, sidewall spacers conforming to said stacked gates;

source regions of a second conductivity type formed within said substrate and adjacent to each of said stacked gates;

a common drain region of a second conductivity type formed within said substrate and defined between each pair of said stacked gates;

channel regions within said substrate lying beneath said stacked gates and defined between said source regions and said common drain region;

a heavily doped implanted region within said common drain region;

a lightly doped implanted region beneath and surrounding said heavily doped implanted region wherein said lightly

doped and said heavily doped implanted regions are smoothly graded doping profiles that extend from said common drain region toward the center of said channel region, wherein said smoothly graded doping profiles are defined by tilt angle impurity implantation and minimal thermal diffusion, and wherein said smoothly graded doping profiles provide minimal inter-memory cell disturb voltage difference.

Please Reinstate Canceled Claim 30 with New Amendments as follows:

30. (REINSTATED AND AMENDED) A stacked gate memory cell pair of Claim 29, wherein said lightly doped implanted region comprises phosphorous ions at a dosage level between about $1x10^{13}$ to $5x10^{13}$ atoms/cm^3.

Please Reinstate Canceled Claim 31 with New Amendments as follows:

31. (REINSTATED AND AMENDED) A stacked gate memory cell pair of Claim 29, wherein said heavily doped implanted region comprises arsenic ions at a dosage level between about $1x10^{15}$ to $5x10^{15}$ atoms/cm^3.

Please Add New Claim 32 as follows:

32. (NEW) A stacked gate memory cell pair of Claim 29, wherein said minimal inter-memory cell disturb voltage difference is about |0.18V|.

Please Add New Claim 33 as follows:

33. (NEW) A stacked gate memory cell pair of Claim 29, wherein said gate oxide layer has a thickness of between about 80 to 95 Å.

Please Add New Claim 34 as follows:

34. (NEW) A stacked gate memory cell pair of Claim 29, wherein said floating gate has a thickness of between about 1000 to 2000 Å.

Please Add New Claim 35 as follows:

35. (NEW) A stacked gate memory cell pair of Claim 29, wherein said inter-gate oxide layer has a thickness of between about 120 to 160 Å.

Please Add New Claim 36 as follows:

36. (NEW) A stacked gate memory cell pair of Claim 29, wherein said control gate has a thickness of between about 1500 to 2000 Å.

Please Add New Claim 37 as follows:

37. (NEW) A stacked gate memory cell pair of Claim 29, wherein said sidewall spacers on said stacked gate have a thickness of between about 1200 to 1500 Å.

Please Add New Claim 38 as follows:

38. (NEW) A stacked gate memory cell pair of Claim 29, wherein said impurity implantation tilt angle is between about 40 to 50 degrees from the horizontal.